IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A computer array, comprising:

a plurality of computers integrated on a unitary substrate, each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of the computers; and wherein,

at least some of the computers are assigned a task different from that assigned to the other computers; and

intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers.

2. (original) The computer array of claim 1, wherein:

each of the computers is assigned a task different from that of the other computers.

3. (previously presented) The computer array of claim 1, wherein:

at least some of the computers are configured for specific input functions, whereby the computers configured for specific input functions can receive data from an external device and communicate the received data to other computers of the array.

4. (previously presented) The computer array of claim 1, wherein:

at least some of the computers are configured for specific output functions, whereby the computers configured for specific output functions can receive data from other computers in the array and communicate the received data to an external device.

5. (original) The computer array of claim 1, wherein:

communication between the computers is asynchronous.

6. (original) The computer array of claim 1, wherein:

communication between the computers is via a plurality of parallel data lines.

7. (previously presented) The computer array of claim 1, wherein:

each of the computers is wired to communicate with at least three of the plurality of computers.

8. (previously presented) The computer array of claim 1, wherein:

the quantity of the computers is 25.

9. (original) The computer array of claim 1, wherein:

the computers are physically arrayed in a 5 by 5 array.

10. (original) The computer array of claim 1, wherein:

at least some of the computers are physically arrayed in a 4 by 6 array.

11. (previously presented) The computer array of claim 1, wherein:

the quantity of the computers along each side of the array is an even number.

12. (previously presented) The computer array of claim 1, wherein:

at least one, but not all, of the computers is in direct communication with an external memory source.

13. (previously presented) The computer array of claim 1, wherein:

at least one of the computers communicates data from an external memory source to at least one other of the plurality of computers.

14. (currently amended) A method for performing a computerized job, comprising:

providing a plurality of computers integrated in a unitary substrate and interconnected via discrete sets of data lines, each set of data lines being dedicated to a particular pair of the computers;

assigning a different task to at least some of the computers; and

executing the tasks on the assigned computers; and wherein

each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

intercommunication between each pair of interconnected computers is carried out through the processors of each pair of interconnected computers.

15. (previously presented) The method of claim 14, wherein:

at least one of the computers is assigned to communicate with an external flash memory.

16. (previously presented) The method of claim 14, wherein:

at least one of the computers is assigned to communicate with an external random access memory.

17. (previously presented) The method of claim 14, wherein:

at least one of the computers accomplishes an input/output function by transferring information between another of the computers and an external device.

18. (original) The method of claim 14, wherein:

one of the computers routes assignments to the remainder of the computers.

19. (currently amended) A computer array, comprising:

a plurality of computers on an integrated circuit chip, each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

a plurality of data connections between the computers, each of the data connections being directly accessible to no more than two of the computers; wherein

at least some of the computers are programmed to perform different functions; and

communication via each of the plurality of data connections is carried out through the processors of the no more than two computers associated with each data connection.

20. (original) The computer array of claim 19, wherein:

the different functions work together to accomplish a task.

21. (original) The computer array of claim 19, wherein:

each of the functions is programmed into the respective computers when the computer array is initialized.

22. (original) The computer array of claim 19, wherein:

communication between the computers is asynchronous.

23. (currently amended) A method for accomplishing a task using a plurality of computers, comprising:

providing the plurality of computers on an integrated substrate and interconnected by data lines, each of the data lines being accessible to no more than two of the computers;

dividing a task into operational components and assigning each of the operational components to one of the computers;

programming at least some of the computers to accomplish each of the operational components; and

executing the operational components on the assigned computers; and wherein

~~wherein~~ each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

communication via each of the data lines is carried out through the processors of the no more than two computers having access to the data line.

24. (previously presented) The method for accomplishing a task of claim 23, wherein:

the operational components are operations used in accomplishing functions of a global positioning system receiver.

25. (original) The method for accomplishing a task of claim 23, wherein:

before the task is begun, programming the computers to accomplish each of the operational components.

26. (original) The method for accomplishing a task of claim 23, wherein:

the computers are arranged in a computer array.

27. – 28. (canceled)

29. (previously presented) The computer array of claim 1, wherein:

the computers operate internally in an asynchronous manner.

30. (previously presented) The computer array of claim 1, wherein:
at least one of the read-only memory and the random access memory in each of the computers is dedicated memory.

31. – 33. (canceled)

34. (previously presented) The computer array of claim 1, wherein:
each of the computers is an independently functioning computer.

35. (previously presented) The computer array of claim 1, wherein:
the computers operate internally in an asynchronous manner; and
the computers communicate with each other asynchronously.

36. (previously presented) The computer array of claim 35, wherein:
at least one of the read-only memory and the random-access memory in each of the computers is dedicated memory.

37. – 39. (canceled)

40. (previously presented) The computer array of claim 1, wherein:
the computers are the same with respect to at least one of structure, circuitry, layout, and operational characteristics.

41. (previously presented) The computer array of claim 40, wherein:
a first one of the computers is directly adjacent a second one of the computers; and
the first one of the computers is a mirror image of the second one of the computers.

42. (currently amended) A computer array, comprising:

a plurality of computers integrated on a substrate, each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

[[and]] a plurality of dedicated data paths connecting pairs of the computers; and wherein

at least some of the computers are assigned a task different from that assigned to the other ~~computers and~~ computers;

at least some of the computers include dedicated memory for the exclusive use of an associated one of the computers; and

intercommunication between each pair of connected computers is carried out through the processors of each pair of connected computers.

43. (currently amended) A computer array, comprising:

a plurality of computers on a unitary substrate, the computers operating asynchronously; and

a plurality of data paths between the computers, each of the data paths facilitating communication between ~~some, but not all,~~ no more than two of the computers; and wherein

at least some of the computers are assigned a task different from that assigned to the other computers; [[and]]

each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

communication via each of the data paths is carried out through the processors of the no more than two computers having access to the data path.

44. (previously presented) The computer array of claim 43, wherein:

the computers communicate with each other asynchronously.

45. (previously presented) The computer array of claim 1, wherein:

the plurality of computers includes at least twenty-four computers.

46. (previously presented) The computer array of claim 1, wherein:
data communicated within the array from a first one of the computers to a second one of the computers must necessarily pass through at least one of the other computers.

47. (previously presented) The computer array of claim 46, wherein:
data communicated within the array from the first one of the computers to the second one of the computers must necessarily pass through at least two of the other computers.

48. (previously presented) The computer array of claim 1, wherein:
at least some of the computers are programmed to function as an input and/or output interface between an external device and other computers of the array.

49. (previously presented) The computer array of claim 1, wherein:
the computer array is a homogeneous array.

50. (currently amended) A computer array, comprising:
a plurality of computers each hard wired to communicate with at least three of the plurality of computers; and
a plurality of data paths connecting the computers, each of the data paths being dedicated to an adjacent pair of the computers; and wherein,
at least some of the computers are assigned a task different from that assigned to the other computers;
each of the plurality of computers is integrated on a unitary substrate; [[and]]
each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and
communication via each of the data paths is carried out through the processors of the adjacent pair of the computers having access to the data path.

51. (previously presented) The computer array of claim 50, wherein:

every one of the computers of the array is hard wired to communicate with at least three of the plurality of computers.

52. (previously presented) The computer array of claim 50, wherein:

every one of the computers is hard wired to at least three data paths; and

each of the three data paths is coupled to a neighboring one of the computers or provides a connection to an external device.

53. (currently amended) A computer array, comprising:

a plurality of computers each hard wired to communicate with at least three of the plurality of computers; and

a plurality of data paths connecting the computers, at least some of the data paths being connected to no more than two of the computers; and wherein,

at least some of the computers are assigned a task different from that assigned to the other computers; and wherein

each of the plurality of computers is integrated on a unitary substrate; [[and]]

each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

communication via each of the data paths connected to no more than two of the computers is carried out through the processors of the no more than two computers connected to the data path.

54. (previously presented) The computer array of claim 53, wherein:

every one of the computers of the array is hard wired to communicate with at least three of the plurality of computers.

55. (previously presented) The computer array of claim 53, wherein:

every one of the computers is hard wired to at least three data paths; and

each of the three data paths is coupled to a neighboring one of the computers or provides a connection to an external device.

56. (currently amended) A computer array, comprising:

at least twenty-four computers integrated in a unitary substrate; and

a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of the computers; and wherein,

each of the computers includes dedicated read-only memory for storing data and instructions, dedicated random access memory for storing data and instructions, and a processor for executing the instructions;

each of the computers is coupled to communicate with at least two of the other computers;

each of the computers operates internally in an asynchronous manner;

each of the computers communicates with the other computers asynchronously; and

communication via each of the data paths is carried out through the processors of the associated pair of computers connected to the data path.

57. (currently amended) A computer array, comprising:

a plurality of computers integrated in a unitary substrate, each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

a plurality of data paths connecting the computers, the data paths being physical, point-to-point links between associated pairs of the computers; and wherein,

at least some of the computers are assigned a task different from that assigned to the other computers; and

communication via each of the data paths is carried out through the processors of the associated pair of computers connected to the data path.

58. (currently amended) A computer array, comprising:

a plurality of independently functioning computers arranged in a matrix on a unitary substrate, each of said plurality of computers having at least two nearest neighbor computers; and

a plurality of sets of interconnecting dedicated data lines, each individual set of said plurality of sets of data lines being disposed between an individual computer and one of its nearest neighbor computers of said plurality of computers or between said individual computer and an external device, some of said plurality of sets of data lines each being connected to no more than two of said plurality of computers;

thereby enabling execution of a plurality of tasks by said plurality of computers, the execution of some of said tasks being different from the execution of others of said tasks; and wherein

each of said plurality of computers communicates with at least three others of said plurality of computers within said matrix; [[and]]

each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

communication via each of said sets of said data lines connected to no more than two of said computers is carried out through said processors of said no more than two of said computers connected to said set of said data lines.

59. (currently amended) A computer array, comprising:

a plurality of independently functioning computers arranged in a matrix on a unitary substrate, each of said plurality of computers having at least two nearest neighbor computers; and

a plurality of sets of interconnecting dedicated data lines, each individual set of said plurality of sets of data lines being disposed between an individual computer and one of its nearest neighbor computers of said plurality of computers;

thereby enabling execution of a plurality of tasks by said plurality of computers, the execution of some of said tasks being different from the execution of others of said tasks; and wherein

each of said plurality of computers is dedicated to communicate with at least three of said plurality of computers within said matrix; [[and]]

each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions; and

communication via each of said sets of said interconnecting dedicated data lines is carried out through said processors of said individual computer and said one of said nearest neighbor computers connected to said set of interconnecting dedicated data lines.

60. (new) The computer array of claim 1, wherein:

a plurality of separate tasks are assigned to the plurality of computers, each of the separate tasks to be performed by a different one of the plurality of computers; and

each separate task accomplishes a function of a subcomponent of a consumer device.